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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,283	04/04/2005	Toshiaki Sasaki	81845.0019	4670

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EXAMINER	
BERDICHEVSKY, MIRIAM	

ART UNIT	PAPER NUMBER
4132	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/530,283	SASAKI ET AL.
	Examiner	**Art Unit**
	MIRIAM BERDICHEVSKY	4132

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _preliminary amendment 6/23/2005_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-15_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-15_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _04 April 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _10/18/2007, 4/4/2005_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

    1. Determining the scope and contents of the prior art.
    2. Ascertaining the differences between the prior art and the claims at issue.
    3. Resolving the level of ordinary skill in the pertinent art.
    4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 4776894 as cited in the IDS) in view of Yamagishi (US 4926230).

As to claim 1, Watanabe teaches a stacked layer type photoelectric conversion device comprising:

- A plurality of conversion units stacked (column 3, lines 60-65) on a substrate (column 3, line 65 to column 4, line 1), each of which includes one conductivity type layer, a photoelectric conversion layer of substantially intrinsic semiconductor and an opposite conductivity type layer in this order from a light incident side (column 4, lines 17-29),

- At least one of the opposite conductivity type layer in a front photoelectric conversion unit arranged relatively closer to the light incident side and the one conductivity type layer in a back photoelectric conversion unit arranged adjacent to the front photoelectric conversion (column 4, lines 29-32) unit includes a silicon composite layer at least in a part thereof (layers 33 and 42, column 4, lines 29-32), and
- The silicon composite layer has an oxygen concentration (column 4, lines 36-48; Examiner notes that a-SiOx is desirable for increasing bandwidth) of more than 25 atomic % and less than 60 atomic % (column 8, lines 36-39) and includes silicon rich phase parts in an amorphous (column 4, lines 36-48) alloy phase of silicon and oxygen.

Watanabe is silent to the composite layer thickness being more than 20 nm and less than 130 nm.

Yamagishi teaches a thickness in the range of 7 nm to 70 nm depending on the dopant concentration to optimize absorption loss (column 2, lines 19-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a layer having a thickness that falls with in the claimed range would increase the active regions of the cells and that the thickness range is dependent on the dopant concentration, as taught by Yamagishi (column 2, lines 19-41).

Regarding claim 3, Watanabe teaches that the silicon rich phase part includes doped amorphous silicon (column 4, lines 36-48).

Regarding claim 8, Watanabe teaches that an optical energy gap of the silicon composite layer is at least 2.2 eV (column 5, lines 55-59). Moreover, a wider bandgap is desirable for improving efficiency by decreasing the absorption of light, as taught by Watanabe (column 1, lines 50-67).

4. Claims 2 and 4-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Yamagishi as applied to claim 1 and further in view of Nakamura (JP 59035016).

Applicant is directed to the above paragraphs for a complete discussion of Watanabe and Yamagishi as applied to claim 1.

Regarding claim 2, Watanabe is silent to that the silicon rich phase part includes a silicon crystal phase.

Nakamura teaches that the silicon rich phase part includes a silicon crystal phase (abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to us the amorphous and crystalline silicon of Nakamura in the composite layer of Watanabe because the solar cell will have the merits of both phases, as taught by Nakamura (abstract). Amorphous silicon has the advantage that it can easily be deposited over large areas while the advantage of crystalline silicon is the increased stability against light exposure.

Regarding claim 4, the silicon composite layer with a thickness of greater than 20 nm but less than 130 nm, a oxygen composition of more than 25 atomic % but less than 60 atomic % and both amorphous and crystalline phases, resulting from the

modification of Watanabe with Yamagishi and Nakamura according to claims 1 and 2, see paragraphs above, will inherently have an reflective index regarding light of 600 nm wavelength is more than 1.7 and less than 2.5.

Regarding claim 5, Watanabe teaches that the substrate is transparent (column 3, lines 60-64). In addition, the silicon composite layer with a thickness of greater than 20 nm but less than 130 nm, a oxygen composition of more than 25 atomic % but less than 60 atomic % and both amorphous and crystalline phases, resulting from the modification of Watanabe with Yamagishi and Nakamura according to claims 1 and 2, see paragraphs above, will inherently have a reflection spectrum of at least one maximal value and at least one minimal value of reflectance in a wavelength range of 500 nm to 800 nm and a difference between the maximal value and the minimal value is at least 1 % because there are no structural differences between the modified device of Watanabe and that of the claimed invention.

Regarding claim 6, the silicon composite layer with a thickness of greater than 20 nm but less than 130 nm, a oxygen composition of more than 25 atomic % but less than 60 atomic % and both amorphous and crystalline phases, resulting from the modification of Watanabe with Yamagishi and Nakamura according to claims 1 and 2, see paragraphs above, will inherently have a dark conductivity of more than 10^{-8} S/cm and less than 10^{-1} S/cm because there are no structural differences between the modified device of Watanabe and that of the claimed invention.

Regarding claim 7, the silicon composite layer with a thickness of greater than 20 nm but less than 130 nm, a oxygen composition of more than 25 atomic % but less than

60 atomic % and both amorphous and crystalline phases, resulting from the modification of Watanabe with Yamagishi and Nakamura according to claims 1 and 2, see paragraphs above, will inherently have an intensity ratio of TO mode peak from the crystalline parts to a TO mode peak from the amorphous parts measure by Raman scattering more than 0.5 and less than 10 because there are no structural differences between the modified device of Watanabe and that of the claimed invention.

Regarding claim 9, the silicon composite layer with a thickness of greater than 20 nm but less than 130 nm, a oxygen composition of more than 25 atomic % but less than 60 atomic % and both amorphous and crystalline phases, resulting from the modification of Watanabe with Yamagishi and Nakamura according to claims 1 and 2, see paragraphs above, will inherently have an energy difference between upper most energy of a photoelectron having suffered interband excitation loss of O1s and peak energy of the O1s photoelectron measured by XPS is at least 2.2 eV because there are no structural differences between the modified device of Watanabe and that of the claimed invention.

5. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Yamagishi as applied to claim 1 and further in view of Yoshida (US 4875944).

Applicant is directed to the above paragraphs for a complete discussion of Watanabe and Yamagishi as applied to claim 1.

Regarding claim 10, Watanabe and Yamagishi are silent to a dopant concentration in the silicon composite layer is in a range from 3×10^{20} cm^{-3} to 1.8×10^{21} cm^{-3}.

Yoshida teaches a dopant concentration in the silicon composite layer is in a range from 3×10^{20} cm^{-3} to 1.8×10^{21} cm^{-3} (column 3, lines 7-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the dopant concentration of Yoshida in the composite layer of Watanabe because the conversion efficiency remains high for a long period of time, as taught by Yoshida (column 3, lines 7-18).

6. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Yamagishi as applied to claim 1 and further in view of Kondo (JP 2002-170973, see machine translation).

Applicant is directed to the above paragraphs for a complete discussion of Watanabe and Yamagishi as applied to claim 1.

Regarding claims 11-12, Watanabe and Yamagishi are silent to the substrate having the silicon composite layer deposited to a part of its total thickness in a plasma CVD reaction chamber is temporarily taken out to expose a surface of the silicon composite layer to the ambient air and then after the substrate is introduced again into a plasma CVD reaction chamber the remaining part of the total thickness of the silicon composite layer is deposited.

Further regarding claim 12, Watanabe and Yamagishi are silent to taking the substrate out from the plasma CVD reaction chamber to the ambient air after at least 60% of the total thickness of the silicon composite layer is deposited.

Kondo teaches having the silicon composite layer deposited to a part of its total thickness in a plasma CVD reaction (¶ [0008]) chamber is temporarily taken out to expose a surface of the silicon composite layer to the ambient air and then after the substrate is introduced again into a plasma CVD reaction chamber the remaining part of the total thickness of the silicon composite layer is deposited and that the substrate is taken out from the plasma CVD reaction chamber to the ambient air after at least 60% (¶ [0008], [0009], [0010], and [0012], where exposure at the end is greater than 60%) of the total thickness of the silicon composite layer is deposited.

It would have been obvious to one of ordinary skill at the time of the invention to use the expose technique of Kondo in the module preparation of Wantanabe because the technique is low in cost and improves the module's stability and resistance to the environment, as taught by Kondo (¶ s [0003] and [0007]]). Furthermore, it would have been obvious to one of ordinary skill in the art to use taking the product out of the CVD as a means for exposing the product to atmosphere (ambient) oxygen and then putting it back in to continue CVD of the following layers.

Regarding claim 13, Watanabe teaches a mixing ratio of doping source gas to silicon source gas for deposition of the silicon composite layer in a plasma CVD reaction chamber is in a range from 0.012 to 0.07 (Table 3, layer 33, PH_3/SiH_4).

7. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (EP 1198014) in view of Watanabe and further in view of Yamagishi.

As to claim 14, Hayashi teaches an integrated type photoelectric conversion device comprising:

- A first electrode layer (3),
- A plurality of conversion units stacked on a substrate, each of which includes one conductivity type layer (4a), and an opposite conductivity type layer (4b) in this order from a light incident side (Figure 2, ¶ [0026]),
- A second electrode (6) layer successively stacked on a substrate separated by a plurality of isolation grooves (21, 22, 23) to form a plurality of photoelectric conversion cells (figure 2, ¶ [0027]), and
- The cells are electrically connected in series (¶ [0030]) with each other.

Hayashi is silent to:

- A photoelectric conversion layer of substantially intrinsic semiconductor, and
- A plurality of stacked photoelectric conversion units each including:
  - At least one of the opposite conductivity type layer in a front photoelectric conversion unit arranged relatively closer to the light incident side and the one conductivity type layer in a back photoelectric conversion unit arranged adjacent to the front photoelectric conversion unit includes a silicon composite layer at least in a part thereof, and

- The silicon composite layer has a thickness of more than 20nm and less than 130nm and an oxygen concentration of more than 25 atomic % and less than 60 atomic % and includes silicon rich phase parts in an amorphous alloy phase of silicon and oxygen.

Watanabe teaches:

- A photoelectric conversion layer of substantially intrinsic semiconductor (column 4, lines 17-32), and
- A plurality of stacked photoelectric conversion units each including:
    - At least one of the opposite conductivity type layer in a front photoelectric conversion unit arranged relatively closer to the light incident side and the one conductivity type layer in a back photoelectric conversion unit arranged adjacent to the front photoelectric conversion unit (column 4, lines 17-32), includes a silicon composite layer at least in a part thereof (layers 33 and 42, column 4, lines 29-32), and
- The silicon composite layer has an oxygen concentration (column 4, lines 36-48; Examiner notes that a-SiOx is desirable for increasing bandwidth) of more than 25 atomic % and less than 60 atomic % (column 8, lines 36-39) and includes silicon rich phase parts in an amorphous (column 4, lines 36-48) alloy phase of silicon and oxygen.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a layer having a thickness that falls with in the claimed range would

increase the active regions of the cells and that the thickness range is dependent on the dopant concentration, as taught by Yamagishi (column 2, lines 19-41).

Hayashi and Watanabe are silent to the composite layer thickness being more than 20 nm and less than 130 nm.

It would have been obvious to one of ordinary skill in the art at the time of the invention to increase the composite layer thickness of the composite layer used in Watanabe because this would increase the active regions of the cells. Furthermore, it has been held that discovering the optimum value of a result effective variable involves only routing skill in art (MPEP, 2144.05, IIB), especially since Yamagishi teaches a thickness in the range of 7 nm to 70 nm depending on the dopant concentration to optimize absorption loss (column 2, lines 19-41).

Regarding claim 15, Hayashi teaches that the first electrode layer (3) is separated into a plurality of regions corresponding to the plurality of photoelectric conversion cells (10) by a plurality of first isolation grooves (21), the plurality of photoelectric conversion unit layers (4a, 4b) and the second electrode layer (6) are separated into a plurality of regions corresponding to the plurality of cells by a plurality of second isolation grooves (22) and a connection groove (23) is provided between the first isolation groove (21) and the second isolation groove to electrically connect the first electrode of one of the cells with the second electrode of its neighboring cell (Figure 2, ¶s [0026], [0027], [0030]).

Correspondence/ Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **MIRIAM BERDICHEVSKY** whose telephone number is (571)270-5256. The examiner can normally be reached on M-Th, 7:30am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on (571) 272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. B./
Examiner, Art Unit 4132

/Jessica L. Ward/
Supervisory Patent Examiner, Art Unit 4132